the plurality of channel areas of each respective second thin film transistor are electrically connected in parallel to each other and arranged separately.

105. The display device according to claim 104, wherein the plurality of channel areas are separated in a direction of the channel width.

106. The display device according to claim 104, wherein the laser annealing is performed to polycrystallize an amorphous semiconductor layer in order to obtain a polycrystalline semiconductor layer.

107. A display device, comprising:

a plurality of pixel electrodes formed on a substrate;

a plurality of first thin film transistors, which are connected to corresponding pixel electrodes among the plurality of pixel electrodes and respectively supply the connected corresponding pixel electrode with a display signal; and

a plurality of second thin film transistors, which configure a driving circuit for driving the plurality of first thin film transistors; wherein,

some of the plurality of second thin film transistors each has a plurality of channel areas formed in a semiconductor layer subjected to laser annealing respectively, and the plurality of channel areas of each respective second thin film transistor are electrically connected in parallel to each other and arranged separately.

108. The display device according to claim 107, wherein the plurality of channel areas are separated in a direction of the channel width.

109. The display device according to claim 107, wherein the laser annealing is performed to polycrystallize an amorphous semiconductor layer in order to obtain a polycrystalline semiconductor layer.

110. A display device, comprising:

a plurality of pixel electrodes formed on a substrate;

a plurality of first thin film transistors, which are connected to corresponding pixel electrodes among the plurality of pixel electrodes and respectively supply the connected corresponding pixel electrode with a display signal; and

a plurality of second thin film transistors, which configure a driving circuit for driving the plurality of first thin film transistors; wherein,

at least one of the plurality of second thin film transistors has a plurality of channel areas formed in a semiconductor layer subjected to laser annealing respectively, and the plurality of channel areas of each respective second thin film transistor are electrically connected in parallel to each other and arranged separately.

111. The display device according to claim 110, wherein the plurality of channel areas are separated in a direction of the channel width.

112. The display device according to claim 110, wherein the laser annealing is performed to polycrystallize an amorphous semiconductor layer in order to obtain a polycrystalline semiconductor layer.

113. A display device, comprising:

a plurality of pixel electrodes formed over a substrate;

a plurality of first thin film transistors, which are connected to corresponding pixel electrodes among the plurality of pixel electrodes and respectively supply the connected corresponding pixel electrode with a display signal; and

a plurality of second thin film transistors, which configure a driving circuit for driving the plurality of first thin film transistors; wherein,

the plurality of second thin film transistors each has a plurality of channel areas formed in a semiconductor layer subjected to laser annealing respectively, and the plurality of channel areas of each respective second thin film transistor are electrically connected in parallel to each other and arranged separately.

114. The display device according to claim 113, wherein the plurality of channel areas are separated in a direction of the channel width.

115. The display device according to claim 113, wherein the laser annealing is performed to polycrystallize an amorphous semiconductor layer in order to obtain a polycrystalline semiconductor layer.

116. A display device, comprising:

a plurality of pixel electrodes formed over a substrate;

a plurality of first thin film transistors, which are connected to corresponding pixel electrodes among the plurality of pixel electrodes and respectively supply the connected corresponding pixel electrode with a display signal; and

a plurality of second thin film transistors, which configure a driving circuit for driving the plurality of first thin film transistors; wherein,

some of the plurality of second thin film transistors each has a plurality of channel areas formed in a semiconductor layer subjected to laser annealing respectively, and the plurality of channel areas of each respective second thin film transistor are electrically connected in parallel to each other and arranged separately.

117. The display device according to claim 116, wherein the plurality of channel areas are separated in a direction of the channel width.

118. The display device according to claim 116, wherein the laser annealing is performed to polycrystallize an amorphous semiconductor layer in order to obtain a polycrystalline semiconductor layer.

119. A display device, comprising:

a plurality of pixel electrodes formed over a substrate;

a plurality of first thin film transistors, which are connected to corresponding pixel electrodes among the plurality of pixel electrodes and respectively supply the connected corresponding pixel electrode with a display signal; and

a plurality of second thin film transistors, which configure a driving circuit for driving the plurality of first thin film transistors; wherein,

at least one of the plurality of second thin film transistors has a plurality of channel areas formed in a semiconductor layer subjected to laser annealing respectively, and the plurality of channel areas of each respective second thin film transistor are electrically connected in parallel to each other and arranged separately.

120. The display device according to claim 119, wherein the plurality of channel areas are separated in a direction of the channel width.

121. The display device according to claim 119, wherein the laser annealing is performed to polycrystallize an amorphous semiconductor layer in order to obtain a polycrystalline semiconductor layer.--